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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,041	03/30/2001	David R. Reuveni	00-413 1496.00064	8448

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LSI LOGIC CORPORATION
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M/S: D-106 PATENT DEPARTMENT
MILPITAS, CA 95035

EXAMINER

TSE, YOUNG TOI

ART UNIT	PAPER NUMBER
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2637

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/822,041

Applicant(s)

REUVENI, DAVID R.

Examiner

YOUNG T. TSE

Art Unit

2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☒ Claim(s) 21-23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 13, 2005 have been fully considered but they are not persuasive.

The Applicant mainly argues that both Chen and Lee do not disclose or suggest an analog circuit configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock as recited in each of the independent claims 1 and 15-16.

The examiner agrees that both Chen and Lee do not use the phrase analog circuit for generating a plurality of samples of an input signal. However, the plurality of samples is already digital signal in the instant application and in both Chen and Lee patents. Notice, some of the circuitry in an analog circuitry includes digital signals. For example, in the instant application, Figure 3 shows the detailed embodiment of the analog circuit 132 as recited in the claims comprising comparators 140a-140n to generate digital signals or bits from 0-bit to 15-bit. Also referring to Figure 5, the digital signals are input to the 16-bit register 160, which clearly operates in digital signals from the output of the analog circuit 132. Therefore, the circuitry used in both Chen and Lee references for generating a plurality of samples of an input signal can be considered as an analog circuit including digital parts.

Claim Objections

2. Claims 7-8 and 18 are objected to because of the following informalities:

In claim 7 (line 4) and claim 18 (line 4), "an accumulated value" should be "a first accumulated value".

In claim 8, lines 2-3), "said accumulated value" should be "said first accumulated value".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6, 13, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen.

Chen (US Patent No. 5,850,422) discloses a clock/data recovery circuit 10 in Figure 1 for recovering a clock signal which is embedded in an incoming data stream.

With respect to claims 1 and 15-17, an analog PLL circuit 12 generates a plurality of phases (P0-P9) of a reference clock to both a data sampler 14 and a clock

multiplexer 16; the data sampler 14 provides a plurality of samples (OP0-OP9) of an input signal generated from an input data 36 through a pulse swallower 22 in response the plurality of phases; and a lead/lag phase detector 18 generates a recovered clock and a re-timed data in response to the input data, the plurality of samples, and the plurality of phases, wherein the recovered clock is aligned with the re-timed data.

With respect to claim 2, the detailed embodiment of the data sampler 14 is shown in Figure 3 which clearly comprising a plurality of sampler circuits for generating the samples OP0-OP9.

With respect to claim 3, clearly, the analog PLL circuit 12 is a PLL circuit and the detailed embodiment is shown in Figure 2.

With respect to claims 6 and 13, the detailed embodiment of the clock multiplexer 16 is shown in Figure 4 which is a serial output circuit.

5. Claims 1-2, 4-5 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al..

Lee et al. (US Patent No. 6,266,799 B1) discloses a data/clock recovery system in Figure 3 for use in a high speed networking transceiver units.

With respect to claims 1 and 15-17, a multiphase clock generator 204 generates a plurality of phases of a reference clock to a four phase sampler circuit 302 via a multiplexer 310; the four phase sampler circuit 302 provides a plurality of samples (D0-D9) of a data stream in response the plurality of phases; and a transition detect and lead-lag decision circuit 304 generates up and down data signals through an up-down counter 306, a decoder 308 and the multiplexer 310 to generate recovered clocks Clk0-

Clk3 in response to the data stream, the plurality of samples, and the plurality of phases, wherein the recovered clocks are aligned with the up and down data signals.

With respect to claim 2, the detailed embodiment of the four phase sampler circuit 302 is shown in Figure 4A which clearly comprising a plurality of sampler circuits for generating the samples D0-D9.

With respect to claims 4 and 5, Figure 5 shows the timing diagram of the data0-data3 and the Clk0-Clk3, clearly, most of the clocks are aligned with a predetermined point of a bit time of the data and Clk0 and Clk3 are aligned with a center of data0 and data1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 7-12, 14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Williams et al. as applied to claims 1 and 16.

Although Lee does not show the detailed embodiments of the transition detect and lead-lag decision circuit 304 as recited in the claimed subject matter of claims 7-12, 14 and 18-20.

Williams et al. (US Patent No. 6,417,698 B1) discloses a linearized digital phase locked loop circuit 100 in Figure 6 for determining a state of a plurality of clock signals.

Wherein the linearized digital phase locked loop circuit 100 comprises a logic block 102 and a control block 104.

The detailed embodiment of the logic block 102 of the linearized digital phase locked loop circuit 100 is shown in Figure 7 which includes the similar circuitry as shown in Lee's data/clock recovery system in Figure 3. The linearized digital phase locked loop circuit 100 comprises a phase detector 122 comprising a register 1 and a coder 130; a filter 124 comprising registers 2 and 3, an enable circuit 132 and an accumulation logic 134; and a switch circuit 126 comprising registers 4 and 5, an increment/decrement logic 136 and a decoder 138 to generate a control signal to control the multiplexer 116.

The control block 104 comprises an edge detector 110 for detecting data DI to generate a data pulse; D-FFs 118a-118n in response to the data and a selected clock to generate DATA; a bandwidth limiter 112 to generate a DATA_VALID; and the multiplexer 116 to generate a PHY_CLK.

With respect to claims 7-10 and 18-20, an accumulated valued is performed by the accumulation logic 134, the increment/decrement of the accumulated values are performed by the increment/decrement logic 136.

With respect to claim 14, since the register1-register5 are shift registers, it is well known to a person skill in the art that a shift register is a first-in-first-out memory.

Therefore, it would have been obvious to one of ordinary skill in the art to include an accumulator circuit and an increment/decrement circuit in Lee's transition detect and lead-lag decision circuit 304 as shown and taught in Williams's logic block to

increment/decrement the accumulated value with a selected phase by a multiplexer in order to align the clock signal by selecting one of the plurality of phases.

Allowable Subject Matter

8. Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

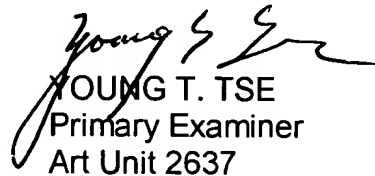
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Thursday and alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The Central FAX Number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


YOUNG T. TSE
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